	L #	Hits	Search Text	DBs	Time Stamp
1	L2	2	("6495883" | "6545316").PN.	US-PGPUB; USPAT; USOCR	2005/06/20 18:24
2	L3	4	("6624470").URPN.	USPAT	2005/06/20 18:29
3	L4	2	("6781197").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/20 18:29
4	L5	5	("5122848" | "6316807" | "6624470" | "6639274" | "6664163").PN.	US-PGPUB; USPAT; USOCR	2005/06/20 18:29
5	L6	1	("6781197").URPN.	USPAT	2005/06/20 18:33
6	L7	1833	(438/270).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/20 18:33

	L #	Hits	Search Text	DBs	Time Stamp
7	L8	102	(438/272).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/20 18:33
8	L9	1868	7 or 8	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/20 18:33
9	L10	723	9 and (gate near2 (oxide or insulator or insulating))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/20 18:34

	L #	Hits	Search Text	DBs	Time Stamp
10	L11	593	10 and trench	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/20 18:34
11	L12	125	11 and drift	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/20 18:34
12	L13	123	12 and drain	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/20 18:34

	L #	Hits	Search Text	DBs	Time Stamp
13	L14	70	13 and ((@ad<"20010530") or (@rlad<"20010530"))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/20 18:35

US-PAT-NO: 5963800

DOCUMENT-IDENTIFIER: US 5963800 A

TITLE: CMOS integration process having vertical channel

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Application Filing Date - AD (1):
19960617

Brief Summary Text - BSTX (7):
The first problem is known as **Drain** Induced Barrier Lowering (DIBL), which, for very short channels exists even without **drain** bias. This effect, results in undesirable high off-state currents, which will have a major contribution to serious power dissipation problems. It also degrades the switching properties (sub threshold current slope) of the devices.

Brief Summary Text - BSTX (11):
However, the DIBL effect remains for these devices, thereby imposing a minimum channel length. This results from the fact that potential barriers built by doping suffer from charge redistribution when a bias is applied, and their maximum value is limited by the band-gap of Si. Also, very short distances between source**/drain** and the delta doped barrier results in a strong field, enhancing band to band tunnelling beyond acceptable levels.

Brief Summary Text - BSTX (12):
U.S. Pat. No. 4,740,826 describes a Vertical Complementary Metal Oxide Semiconductor (CMOS) inverter fabricated by forming a layer of P-type material on the surface of an N+-type substrate followed by formation of an N+ layer, a P+ layer, an N-layer and a P+ layer. A **trench** is then etched along one side of the stack thus formed and a connector is formed to the middle P+ and N+ layers. In addition, another **trench** is formed to create a **gate insulator and**

a- gate.
There is only homojunction between the several layers.

Brief Summary Text - BSTX (16):
U.S. Pat. No. 4,236,166 describes a Vertical Field Effect Transistor which includes a relatively wide bandgap, lowly doped active layer epitaxially grown on, and substantially lattice matched to, an underlying semiconductor body portion. A mesa of lower bandgap material is epitaxially grown on and substantially lattice matched to the active layer. A source electrode is formed on a bottom major surface of the semiconductor body portion, a **drain** electrode is formed on the top of the mesa, and a pair of gate electrode stipes are formed on the active layer adjacent both sides of the mesa.

Brief Summary Text - BSTX (21):
b) Parasitic capacitances coming from extensive gate overlap of highly doped regions. The gate fully overlaps the source and **drain** (which is something that doesn't happen with planar transistors). This capacitance can be significative since "thick" source and **drain** layers should be provided for minimization of the series resistance.

Brief Summary Text - BSTX (36):
One embodiment of the present invention is a silicon-germanium based Vertical MISFET device comprising in a stack of several layers including at least a source layer, a channel layer, and a **drain** layer.

Brief Summary Text - BSTX (40):
c) A gate is overlapping, preferably essentially at a right angle, at least partially the source, the channel and the **drain** layers with an insulate layer therebetween.

Brief Summary Text - BSTX (41):
In the case of a PMOS device, the **drain** is made of a highly p-type doped material which is preferably the same material as the channel material. In

this embodiment, the channel is an undoped material and the source comprises at
least a double layer consisting of an undoped or lowly p-type doped region and
a highly p-type doped region, both made of a second material which has a
valence band edge with a lower potential energy than the valence band edge of
the channel material.

Brief Summary Text - BSTX (43):
a) The **drain** comprises a highly doped p++ layer preferably Si layer.

Brief Summary Text - BSTX (46):
The present invention also relates to NMOS devices. In this embodiment, the
drain is made of a highly n-doped material preferably the same material as the
channel material, the channel is an undoped material, and the source comprises
at least a double layer consisting of an undoped or lowly n-type doped region
and a highly n-type doped region, both made of a second material which has a
conduction band edge with a lower potential energy than the conduction band
edge of the channel material.

Brief Summary Text - BSTX (48):
a) The **drain** comprises a highly doped n++ layer preferably Si layer.

Brief Summary Text - BSTX (52):
a) The **drain** comprises a highly doped n++ layer (preferably Ge).

Brief Summary Text - BSTX (56):
Using silicon epitaxial compatible materials, the PMOS device has the
following configuration: the **drain** comprises a p++ silicon layer; the channel
comprises an undoped silicon layer, the source comprises undoped
silicon-germanium layer and a p++ silicon-germanium layer.

Brief Summary Text - BSTX (57):
Using the same material, the NMOS device is less straightforward due to the
small conduction band off-set of SiGe layers drained to Si wafer. Such can be
circumvented by the use of a Si.sub.0.5 Ge.sub.0.5 virtual substrate.

In this
case, the NMOS has the following configuration: the **drain** comprises an n++ Ge
layer; the channel comprises an undoped Ge layer; the source comprises undoped
or lightly n-type doped SiGe layer and an n++ SiGe layer.

Brief Summary Text - BSTX (62):
In the case of a CMOS inverter, the PMOS source is grounded, NMOS source is
at -VSS, Input signal is put at the common gate contact, and Output signal is
taken at the common **drain** contact.

Brief Summary Text - BSTX (63):
For pass transistors, a Control signal is put at the gate of a single MOS,
to allow or forbid the access of the **drain** to the signal at the source. Quite
often the control signal is a clock. So, for pass transistors, the terminal of
the PMOS must be fully independent of the terminals of the NMOS and vice-versa.

Brief Summary Text - BSTX (64):
According to the present invention, a surrounding gate is provided common to
the whole stack of the several devices. Preferably such stack of devices also
has a **drain** contact common to all the stacked devices. Preferably the **drain**
contact is made inside the perimeter of the stack of the device.

Brief Summary Text - BSTX (66):
The present invention also relates to a process integration for Vertical
MISFET devices, each of the MISFET devices comprising a stack of several layers
including at least a source layer, a channel layer and a **drain** layer and having
a surrounding **gate and insulator** overlapping at least partially the several
layers of the MISFET device wherein:

Brief Summary Text - BSTX (69):
c) other patterning steps are used to make contact to the source and to the
drain of each Vertical MISFET device possibly stacked.

Brief Summary Text - BSTX (70):

Preferably, the patterning step used in order to make the contact to the **drain** of the devices is performed in order to have said **drain** common to several stacked devices made inside the perimeter of the stacked device(s).

Brief Summary Text - BSTX (81):
h) Mask 3: (Common) **Drain** Contact Holes

Brief Summary Text - BSTX (87):
The present invention also relates to RAM circuits comprising memory cells and a logic circuitry. According to a first preferred embodiment, each of the memory cells comprises at least one Vertical MISFET device having itself a stack of several layers comprising a source layer, a channel layer and a **drain** layer and a capacitor on the top of the stack of several layers of the Vertical MISFET device.

Brief Summary Text - BSTX (93):
c) a gate which is overlapping, preferably essentially at right angle, at least partially the source, the channel, and the **drain** layers with an insulate layer there between.

Drawing Description Text - DRTX (2):
FIG. 1 represents the band structure and the electrochemical potential in function of the distance (from the source to the **drain**) for a PMOS device according to the present invention under the three following bias conditions:

Drawing Description Text - DRTX (4):
drain bias (FIG. 1b),

Drawing Description Text - DRTX (5):
drain and gate bias (FIG. 1c).

Detailed Description Text - DETX (3):
FIG. 1 represents the band structure and the electrochemical potential as functions of distance (from source to **drain**) for a PMOS device. The plots were obtained with a commercial device simulator (TMA's Medici with heterojunction

MOSFET (without contact) can be much smaller than the footprint of planar
MOSFETs. In vertical MOSFETs, the regions of source, channel and **drain** are
stacked upon each other, effectively having the footprint of one. This is true
as long as individual contacts to the regions of each MOSFET in the circuit are
not required.

Detailed Description Text - DETX (333):
If the RAM architecture required individual contacts to the source, **drain**
and gate of each transistor, there would be no area advantage of vertical over
planar MOSFETs. With a "wide bit" arrangement, Wordline contact is made
simultaneously to several transistors, and that is what gives the advantage to
vertical MOSFETs. The "wider" the bit, the larger the advantage.

Detailed Description Text - DETX (340):
Formation of 1st **Trenches**;

Detailed Description Text - DETX (341):
Formation of 2nd **Trenches** (perpendicular to 1st ones);

Detailed Description Text - DETX (342):
Formation of Surrounding **Gate Insulator**;

Detailed Description Text - DETX (361):
8) Damageless (dry or wet) etch of crystalline silicon layers (**Drain** &
Channel), stopping on the bottom highly doped n++ layer (Source).

Detailed Description Text - DETX (386):
26) CVD and etchback of oxide, to make spacers. This thickness, being
larger than the stepper's overlay accuracy, will define the width of the **trench**
between the gates of the different cells.

Detailed Description Text - DETX (392):
30) Cobalt (or Nickel) salicidation of the poly gate electrode and of the
top of the poly plugs. These silicides can be formed at low temperature
(300.degree. C. for Ni), and cannot be dry etched. It might be difficult to
remove the unreacted metal from the bottom of the **trenches**. It